

### **REMARKS**

Applicants thank the Examiner for the courtesy of an interview on September 9, 2004, to discuss this application. An interview summary is being filed herewith. At this interview, Applicants generally discussed the claims and distinguished the claims from the prior art.

Claims 1-27 are currently pending in this application. In the last Office Action, claims 8, 9-11 were objected to because of an informality. Claims 1-6 and 19-23 were rejected under 35 U.S.C. 102(b) as being anticipated by Heffner et al. (U.S. Patent No. 3,921,079). Claims 7-11 were rejected under 35 U.S.C. 103(c) as being unpatentable over Heffner. Method claims 12-18 and 24-27 were rejected "based on the rejection of the apparatus claims."

While Applicants do not necessarily agree with the rejections in the last office action, this Response cancels claims 2, 6 and 27, amends claims 1, 3-4, 7-8, and 24, and adds new claims 28-30 to clarify these claims and to expedite prosecution of this application.

#### **1. Reasons why the rejection of claims 1, 3, 4-5 and 7 should be withdrawn**

Claims 1, 3 and 4-5 were rejected as anticipated by Heffner, and claim 7 was rejected as obvious over Heffner. Applicants respectfully request the withdrawal of these rejections for the following reasons.

As amended, claim 1 recites a circuit that comprises a delay adjustment input "wherein the adjustment of the timing of the clock signal at said one output is to adjust the timing of the clock signal at outputs that follow said one output in the multistage clock." Similarly, claim 4 recites a circuit with a plurality of delay adjustment "wherein each of the delay adjustment blocks varies the delay between an associated clock output and clock outputs that follow that output in the sequential order."

Applicants submit that Heffner does not disclose or suggest a circuit with a delay adjustment input “wherein the adjustment of the timing of the clock signal at said one output is to adjust the timing of the clock signal at outputs that follow said one output in the multistage clock,” as recited in claim 1, or with a plurality of delay adjustment “wherein each of the delay adjustment blocks varies the delay between an associated clock output and clock outputs that follow that output in the sequential order,” as recited in claim 4.

To the contrary, Heffner discloses a “multi-phase clock distribution system having a plurality of outputs each of which is individually adjustable in phase.” See col. 1, lines 9-11 (emphasis added). Thus, as shown in FIG. 1, Heffner has a plurality of phase shift adjust means (for example, block 24) which each have an output that is coupled to a single output (for example, output A1). Adjusting of one of the clock outputs in Heffner would not adjust “clock outputs that follow that output” as recited in claims 1 and 4.

Applicants also note that there is no evidence of a motivation to modify the prior art references to obtain the claimed invention. See, e.g., *In re Zurko*, 258 F.3d 1379, 1368 (Fed. Cir. 2001) (holding that an Examiner must “point to some concrete evidence in the record” of a motivation to combine or modify the references to support an obviousness rejection).

For at least these reasons, claims 1 and 4 are believed to be patentable. Claims 3, 5 and 7 depend from one of claims 1 and 4 and are patentable for at least the same reasons as claims 1 and 4, as well as for additional limitations contained therein. New claims 27-30 also depend from claim 1 and are patentable for at least the same reason as claim 1.

## **2. Reasons why the rejection of claims 8-11 should be withdrawn**

Claims 8-11 were rejected as anticipated by Heffner, and claim 7 was rejected as obvious over Heffner. Applicants respectfully request the withdrawal of these rejections for the following reasons.

Amended claim 8 recites a circuit having a plurality of “first delay blocks” and a plurality of “second delay blocks,” wherein “each of the first delay blocks is on a single path from the clock input to a clock output” and wherein “each of the second delay blocks is on one path from the clock input to one of the clock outputs and is on another path from the clock input to another of the clock outputs.” For example, as shown in FIG. 2 of the present application, third stage delay block 233 is on a single path from clock input 112 to third stage clock output 233 (that is, from input 112 to first common delay block 211 to second common delay block 212 to third stage delay block 223 to third stage clock output 233). In addition, second common delay block 212 is on one path from the clock input to one of the clock outputs (the same path described above in the previous sentence) and on another path from the clock input to another of the clock outputs (that is, from input 112 to first common delay block 211 to second common delay block 212 to fourth stage delay block 224 to fourth stage clock output 234).

Applicants submit that Heffner does not disclose these limitations of claim 8 at least for the following reasons. First, Heffner’s circuits 70-76, which were relied upon to reject claim 8 in the last Office Action, do not constitute “delay blocks” in that circuits 70-76 are each “state decoder counting means.” Moreover, even if circuits 70-76 were delay blocks, these circuits are not each part of a path from the input to one output and a path from that input to another output, as required of the “second delay blocks” in claim 8.

Finally, Applicants submit that there is no evidence of a motivation to modify the prior art references to obtain the claimed invention. See, e.g., *In re Zurko*, 258 F.3d at 1368 (holding that an Examiner must “point to some concrete evidence in the record” of a motivation to combine or modify the references to support an obviousness rejection). The last Office Action stated that “one of ordinary skill in the art would have recognized that it would have been obvious for the delay adjustment block to connect to the output of one of the second delay adjustment blocks because it would increase the accuracy for determining the amount of delay.” See Office Action at ¶ 16. However, not only is there no evidence in the record of even a suggestion that such a proposed arrangement “would increase the accuracy for determining the amount of delay,” there is no evidence

that a person or ordinary skill in the art would be aware of such a supposed advantage. Because there is no evidence upon which to base a motivation to combine, Applicants submit that the rejection of claim 8 should be withdrawn.

For at least these reasons, claim 8 is believed to be patentable. Claims 9-11 depend from claim 8 are patentable for at least the same reasons as claim 8, as well as for additional limitations contained therein.

### **3. Reasons why the rejection of claims 12-23 should be withdrawn**

Claims 12-23 were rejected as obvious over Heffner. Applicants respectfully request the withdrawal of these rejections for the following reasons.

Claim 12 recites a method of providing a plurality of delayed clock signals, the method including delaying a received clock signal using a second pair of inverters to provide a second clock output signal that is delayed by approximately a time  $t$  from the first clock output signal, delaying the received clock signal using a first delay block to “provide a first internal clock signal that is delayed by approximately time  $2t$  from the received clock signal,” and “delaying the first internal clock signal using a third pair of inverters to provide a third clock output signal that is delayed by approximately time  $t$  from the second clock output signal.”

Claim 19 recites a circuit that includes a first chain of two inverters, a second chain of two inverters, a third chain of two inverters, and a “fourth chain of two inverters having an input connected to the output of the third chain of inverters and having an output connected to a third clock output.”

The Office Action states that Heffner teaches a circuit that comprises “a plurality of chain of two inverters (inverters 17-11 of FIG. 1 and inverter 98, shown in FIG. 4, in each of circuits 70-76).” See Office Action ¶ 17.

As to claim 12, even if one assumed that items 17 and 98 in Heffner constitute a chain of inverters, Heffner does disclose using chains of inverters to provide a first internal clock signal that is “delayed by approximately time  $2t$  from the received clock signal” or “delaying the first internal clock signal using a third pair of inverters to provide a third clock output signal that is delayed by approximately time  $t$  from the second clock output signal,” where time  $t$  is the delay between the first output signal and the second clock output signal, as is recited in claim 12.

As to claim 19, even if one assumed that items 17 and 98 in Heffner constitute a chain of inverters, Heffner does disclose a “fourth chain of two inverters having an input connected to the output of the third chain of inverters and having an output connected to a third clock output,” as is recited in claim 19.

For at least these reasons, claims 12 and 19 are believed to be patentable. Claims 13-18 and 20-23 depend from one of claims 12 or 19 and are patentable for at least the same reasons as claim 12 and 19, as well as for additional limitations contained therein.

#### **4. Reasons why the rejection of claims 24-26 should be withdrawn**

Claims 24-26 were rejected as obvious over Heffner. Applicants respectfully request the withdrawal of these rejections for the following reasons.

Claim 24 recites a method of adjusting the delay of a clock signal in a multistage clock, the method including setting a first storage element “which will later cause the input of a clock adjustment signal to a clock delay circuit and thereby create a contention current to reduce the delay between said one stage of the multistage clock and said following stage.” Among other things, Heffner does not disclose or suggest setting a storage element to “create a contention current” that is to reduce the delay between clock stages, as recite in claim 24. As noted above, in order to reject a claim as obvious, an Office Action must “point to some concrete evidence in the record” of a

motivation to combine or modify the references to support an obviousness rejection. *See, In re Zurko*, 258 F.3d at 1368. Here, the Office Action has not provided any explanation of a motivation to modify Heffner to obtain the method recited in claim 24, let alone "concrete evidence in the record" of such a motivation.

For at least these reasons, claim 24 is believed to be patentable. Claims 25-26 depend from claim 24 and are patentable for at least the same reasons as claims 24, as well as for additional limitations contained therein.


## 5. Conclusion

Applicants respectfully request entry of the above amendments and favorable action in connection with this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600. The Examiner is invited to contact the undersigned at (202) 220-4310 to discuss any matter concerning this application.

Respectfully submitted,

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